REMARKS

Applicant respectfully requests reconsideration of this application in view of the foregoing amendments and the following remarks.

Claim Status

Claims 1-20 are pending in this application and have been rejected by the Examiner. Claims 1 and 11-20 are herein amended. No new matter has been added by these amendments.

Rejections to the Specification Under 35 U.S.C. § 112

Claims 1-20 have been rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention.

With regard to independent claims 1 and 11, the Examiner indicated that "the phrase 'a test bed adapted to receive ... wafers ...' [c]annot be understood." More specifically, the Examiner stated that it is "not clear how hardware (wafers) can be received." Applicant respectfully disagrees.

Applicant directs the Examiner to page 6, lines 6-17 of the specification, for a description of the "test bed adapted to receive ... wafers." As described, for example, on page 6, lines 12-15, a tester 10 includes, inter alia, "a test bed adapted to receive a number of wafers ..." In other words, the tester 10 includes a test bed, which is capable of having a semiconductor wafer positioned thereon, so that the wafer can be tested by the tester 10. Thus, Applicant believes that the "a test bed adapted to receive a number of wafers ..." is clearly defined in the specification and is not indefinite. Accordingly, reconsideration and withdrawal of this rejection is respectfully requested.

Claims 12 and 14 have been rejected for having improper claim dependencies. Claims 12 and 14 have been amended to depend from claims 11 and 13, respectively. Based on such amendments, reconsideration and withdrawal of this rejection is respectfully requested.

Claims 13 and 15-18 have been amended to change their claim dependencies. They have not been amended in response to a rejection raised by the Examiner.

The Examiner has rejected claims 19 and 20 for containing elements lacking antecedent basis. Applicant has made various amendments to claims 19 and 20 to correct these deficiencies. Accordingly, reconsideration and withdrawal of this rejection is respectfully requested.

The Examiner also rejected claims 2-10, 13, and 15-18 "because they depend from claims 1 and 11 and have the same problems of indefiniteness." Based on the discussion above with respect to claims 1 and 11, from which claims 2-10, 13, and 15-18 depend, reconsideration and withdrawal of this rejection is respectfully requested.

Rejections Under 35 U.S.C. § 103(a)

Claims 1-20 have been rejected under 35 U.S.C. § 103(a) as being anticipated by U.S. Patent No. 6,000,048 (Krishna) in view of what would have been obvious to one of ordinary skill in the art at the time the invention was made.

As will be explained below, Applicant respectfully submits that independent claims 1 and 11 as amended are neither taught, disclosed nor suggested by Krishna alone or in view of what would have been obvious to one of ordinary skill in the art at the time the invention was made.

The present invention as recited in amended claim 1 is directed to a method for testing a memory that comprises, inter alia, providing semiconductor wafers having one or more semiconductor chips thereon that comprise one or more segments, each segment comprising one or more memory cells, and a testing apparatus for testing the semiconductor wafers. The method further comprises:

> receiving one or more test commands;
> constructing a test sequence of one or more commanded tests from said test commands;
> constructing at least one header comprising identification information for at least one of said wafer, chip, segment, and memory cell, wherein said identification information comprises location information for at least one of said wafer, chip, segment, and memory cell, and a test identifier for the test sequence to be applied to at least one of said wafer, chip, segment, and memory cell;
> testing at least one of said wafer, chip, segment, and memory cell with the test sequence using one or more test patterns generated by said test pattern generator;
> collecting the results of said testing and passing them to a display device;
> passing said identification information to said display device;
> constructing and displaying a graphical representation of said test results using said identification information.

In contrast to the present invention, Krishna discloses a built-in self test (BIST) for an integrated circuit (IC) including a large logic section, a large dynamic random access memory (DRAM), and a smaller static RAM (SRAM). The IC of Krishna includes circuitry to enable the IC to conduct a BIST of the DRAM. During the BIST, test data is provided to the DRAM by a data register 74, and words of the DRAM that are arranged, for example, in rows and columns, are accessed by two 9-bit address registers 70 and 72, which provide the x and y-addresses of the DRAM.

Krishna, however, does not disclose constructing at least one header comprising "identification information ... wherein said identification information comprises location information for at least one of said wafer, chip, segment, and memory cell, and a test identifier for the test sequence to be applied to at least one of said wafer, chip, segment, and memory cell."

As such, Applicant believes that the invention as recited in independent claims 1 and 11 is patentable over the cited art of record because Krishna taken alone or in combination with what would have been obvious to one having ordinary skill in the art at the time the invention was made does not teach, disclose nor suggest the invention as claimed.

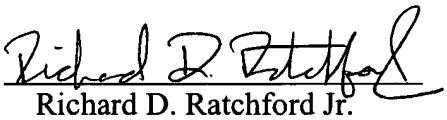
Dependent Claims

Applicant has not independently addressed the rejections of the dependent claims because Applicant submits that, in view of the amendments to the claims presented herein and, for at least similar reasons as why the independent claims from which the dependent claims depend are believed allowable as discussed, *supra*, the dependent claims are also allowable. Applicant however, reserves the right to address any individual rejections of the dependent claims should such be necessary or appropriate.

CONCLUSION

Accordingly, Applicant submits that the claims as herein presented are allowable over the prior art of record, taken alone or in combination, and that the respective rejections be withdrawn. Applicant further submits that the application is hereby placed in condition for allowance which action is earnestly solicited.

Respectfully submitted,

By: 

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